AMENDMENTS TO THE CLAIMS:

The below listing of claims replaces all previous listings and versions of claims in this application:

1. – 11. (Canceled)

12. (Currently Amended) A PN code hopping device as in claim ~~11~~ 13 wherein the at least one memory device further comprises:

a N-x-Spreading Factor (SF) storage capacity, where N is an integer equal to a number of chips and SF is equal to N/symbol; and

N-parallel outputs.

13. (Currently Amended) A PN code hopping device ~~as in claim 11 wherein the at least one memory device further comprises~~ comprising:

at least one memory device, wherein the at least one memory device comprises:

a plurality of time limited PN codes;

an addressable multiplexer, wherein the addressable multiplexer is coupled to the at least one memory device;

an address generator, wherein the address generator is coupled to the addressable multiplexer;

a N-x-Spreading Factor (SF) storage capacity, where N is an integer equal to a number of chips and SF is equal to N/symbol;

a universal serial bus (USB) port; and

a serial to N-parallel converter.

14. (Currently Amended) A PN code hopping device as in claim ~~11~~ 13 wherein the addressable multiplexer comprises a N:1 multiplexer where N is an integer equal to a number of chips associated with one of the plurality of time limited PN codes.

15. (Currently Amended) A PN code hopping device as in claim ~~11~~ 13 wherein the address generator comprises a look-up-table (LUT).

16. (Currently Amended) A PN code hopping device as in claim ~~11~~ 13 wherein the address generator comprises a shift register.

17. (Currently Amended) A PN code hopping device as in claim ~~11~~ 13 wherein the address generator comprises:

an up-down counter; and

a look-up-table, wherein the look-up-table is coupled to the up-down counter.

18. (Previously Presented) A pseudo noise (PN) code hopping system for mitigating cross-correlation interference between Direct Sequence-Code Division Multiple Access (DS-CDMA) users, the system comprising:

a first PN code hopping module, wherein the first PN code hopping module comprises:

a first memory device;

a first addressable multiplexer, wherein the addressable multiplexer is coupled to the first memory device;

a first address generator, wherein the first address generator is coupled to the first addressable multiplexer;

a second PN code hopping module, the second PN code hopping module is coupled to the first PN code hopping module, wherein the second PN code hopping module comprises:

a second memory device;

a second addressable multiplexer, wherein the addressable multiplexer is coupled to the second memory device; and

a second address generator, wherein the second address generator is coupled to the second addressable multiplexer.

19. (Currently Amended) A PN code hopping system as in claim 18 wherein the first memory device comprises:

a first modulation matrix ~~M~~ of size L x L, where L is an integer equal to SF_{max}/SF_{min}, and where SF_{max} is a maximum spread factor and SF_{min} is a minimum spread factor and where SF_{max} and SF_{min} are integers, wherein the first modulation matrix comprises a first set of time limited PN codes; and

L parallel outputs.

20. (Previously Presented) A PN code hopping system as in Claim 18 wherein the first addressable multiplexer comprises a L:1 multiplexer.

21. (Original) A PN code hopping system as in Claim 18 wherein the first address generator comprises:

a first up-down counter; and

a first look-up-table (LUT), the first LUT coupled to the first up-down counter.

22. (Original) A PN code hopping system as in Claim 18 wherein the first address generator comprises a first shift register.

23. (Currently Amended) A PN code hopping system as in claim 18 wherein the second memory device comprises:

a second modulation matrix ~~(M)~~ of size P x nP, where $P = SF_{max}/L$, where L is an integer equal to SF_{max}/SF_{min}, where SF_{max} is the maximum spread factor and SF_{min} is the minimum spread factor, where SF_{max} and SF_{min} are integers, a code order number n is equal to a PN order, and wherein the second modulation matrix comprises a second set of time limited PN codes; and

P parallel outputs.

24. (Previously Presented) A PN code hopping system as in Claim 23 wherein the second addressable multiplexer comprises a P:1 multiplexer.

25. (Original) A PN code hopping system as in Claim 18 wherein the second address generator comprises:

a second up-down counter; and

a second look-up-table (LUT), the second LUT coupled to the second up-down counter.

26. (Original) A PN code hopping system as in Claim 18 wherein the second address generator comprises a second shift register.

27. – 29. (Canceled)